

# REALTEK

## RTL8225

### IEEE 802.11g WLAN RF TRANSCEIVER

### DATASHEET

Rev. 0.9

08 May 2005

Track ID: JATR-1076-21



Realtek Semiconductor Corp.

No. 2, Industry E. Rd. IX, Science-Based Industrial Park, Hsinchu 300, Taiwan

Tel: +886-3-5780211 Fax: +886-3-5776047

[www.realtek.com.tw](http://www.realtek.com.tw)

**COPYRIGHT**

©2005 Realtek Semiconductor Corp. All rights reserved. No part of this document may be reproduced, transmitted, transcribed, stored in a retrieval system, or translated into any language in any form or by any means without the written permission of Realtek Semiconductor Corp.

**DISCLAIMER**

Realtek provides this document “as is”, without warranty of any kind, neither expressed nor implied, including, but not limited to, the particular purpose. Realtek may make improvements and/or changes in this document or in the product described in this document at any time. This document could include technical inaccuracies or typographical errors.

**TRADEMARKS**

Realtek is a trademark of Realtek Semiconductor Corporation. Other names mentioned in this document are trademarks/registered trademarks of their respective owners.

**USING THIS DOCUMENT**

This document is intended for the hardware and software engineer’s general information on the Realtek RTL8225 IEEE 802.11b/g WLAN RF Transceiver chip.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide. In that event, please contact your Realtek representative for additional information that may help in the development process.

**REVISION HISTORY**

Revision	Release Date	Summary
0.9	2005/05/08	Preliminary release.

---

## Table of Contents

---

<b>1. General Description &amp; Features .....</b>	<b>1</b>
<b>3. Block Diagram .....</b>	<b>2</b>
<b>4. Pin Assignments .....</b>	<b>3</b>
<b>5. Pin Descriptions .....</b>	<b>4</b>
<b>6. Serial Interface .....</b>	<b>6</b>
6.1. READ/WRITE ALL REGISTERS .....	6
6.2. READ REGISTER DATA TIMING .....	6
6.3. HIGH SPEED SERIAL INTERFACE TIMING .....	7
<b>7. Characteristics .....</b>	<b>8</b>
7.1. RF CHIP OPERATION MODE CONTROL .....	8
7.2. DC CHARACTERISTICS .....	8
7.3. AC CHARACTERISTICS .....	9
7.4. MEASUREMENT RESULTS .....	10
<b>8. Mechanical Dimensions .....</b>	<b>11</b>
<b>9. Ordering Information .....</b>	<b>12</b>

---

---

## List of Tables

---

Table 1.	Pin Descriptions .....	4
Table 2.	Read/Write All Registers .....	6
Table 3.	High Speed Serial Interface Timing.....	7
Table 4.	RF Chip Operation Mode Control .....	8
Table 5.	DC Specification.....	8
Table 6.	AC Specification.....	9
Table 7.	Ordering Information.....	12

---

## List of Figures

---

Figure 1.	Block Diagram .....	2
Figure 2.	Pin Assignments .....	3
Figure 3.	Read/Write All Registers.....	6
Figure 4.	Read Register Data Timing .....	6
Figure 5.	High Speed Serial Interface Timing.....	7
Figure 6.	Measurement Results .....	10
Figure 7.	Receiver EVM versus RF input power. EVM=-22.5dB@Pin=-76dBm .....	10

---

## 1. General Description & Features

- IEEE 802.11b/g Zero-IF RF Transceiver
- Building Synthesizer LC Auto Calibration
- Building RX Low Pass Filter RC Auto Calibration
- Fast 80MHz Series Interface control transmit and receive PGA
- Transceiver multi-mode control by 3-wire interface or shut down transceiver by external power down pin
- Whole chip ESD Protection Circuits
- Self power on reset
- On-chip Oscillator
- Synthesizer clock source selectable

### 3. Block Diagram

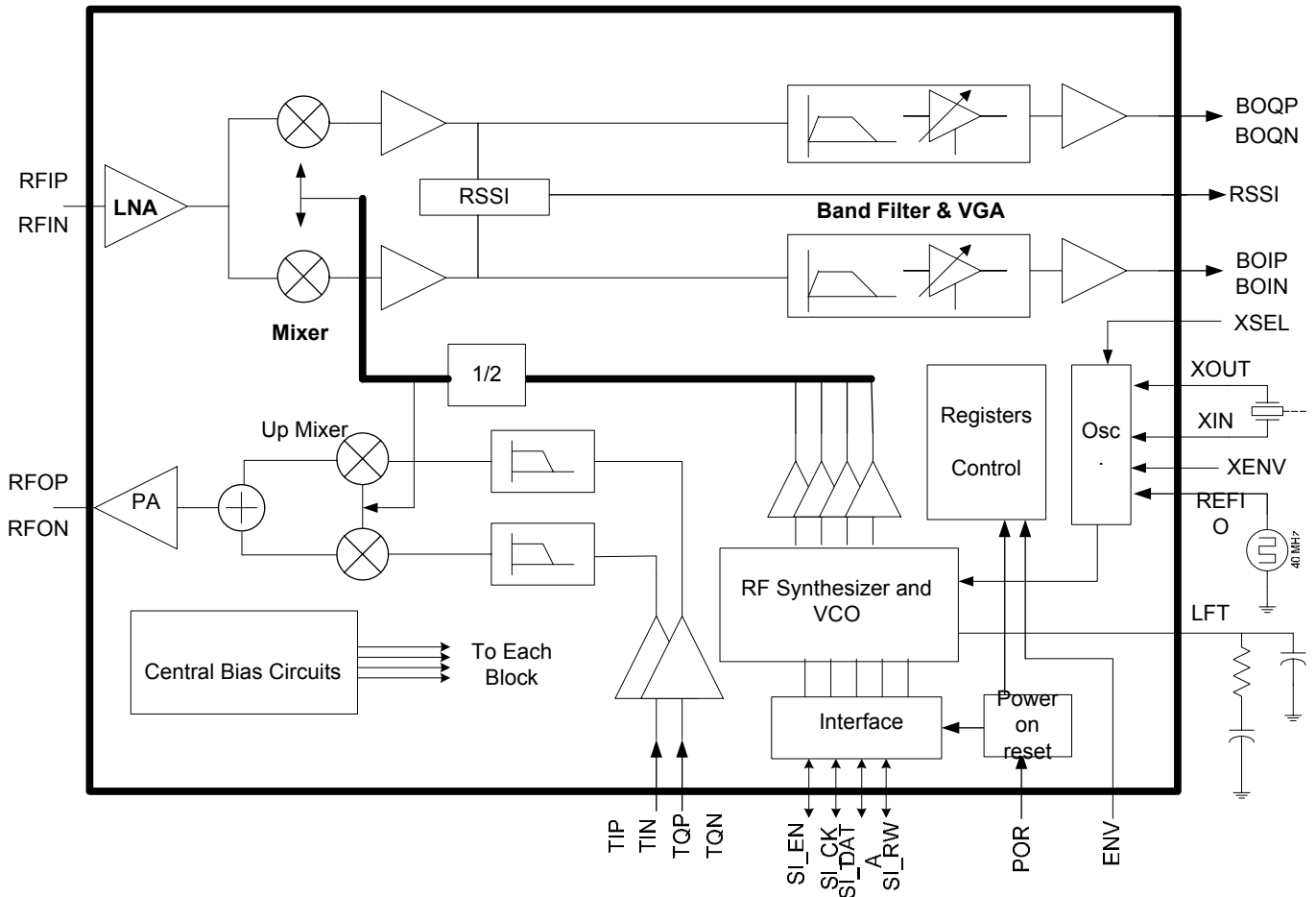


Figure 1. Block Diagram

## 4. Pin Assignments

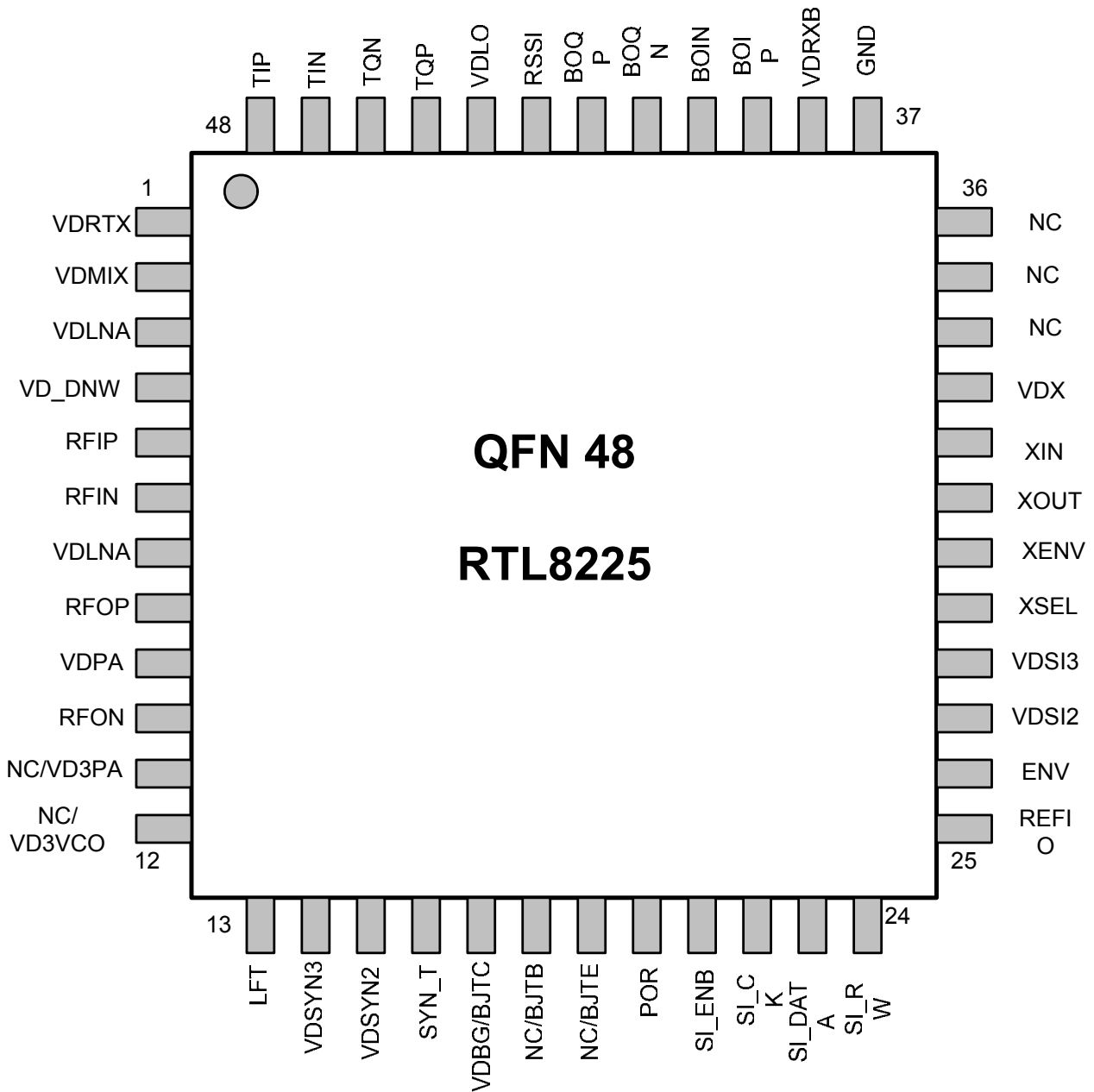


Figure 2. Pin Assignments

## 5. Pin Descriptions

PD: VDD voltage power

PS: GND

AI : Analog input pin

AO : Analog output pin

RF : RF signal I/O pin

DI : Digital Input pin

DO : Digital Output pin

DIO : Digital I/O pin

**Table 1. Pin Descriptions**

Pin	Pin Name	Function	Pad Tape	DC
1	VDRTX	Vdd of RX RSSI/Buffer/Bias, TX LPF/Bias, LO Buffer	PD	1.8V
2	VDMIX	Vdd of RX/TX Mixer and Mixer bias	PD	1.8V
3	VDLNA	Vdd of LNA	PD	1.8V
4	VD_DNW	deep N Well Vdd Bias	PD	1.8V
5	RFIP	RX RF Input	RF	
6	RFIN	RX RF Input	RF	
7	VDLNA	Vdd of LNA	PD	1.8V
8	RFOP	TX PA driver output	RF	
9	VDPA	Vdd of PA	PD	2.8V
10	RFON	TX PA driver output	RF	
11	NC/VD3PA	Reserved for future use	PD	3.3V
12	NC/VD3VCO	Reserved for future use	PD	3.3V
13	LFT	loop filter output	AO	
14	VDSYN3	2.8V Vdd for Synthesizer	PD	2.8V
15	VDSYN2	1.8V Vdd for Synthesizer	PD	1.8V
16	SYN_T	Synthesizer testing pin	RF	
17	VDBG/BJTC	1.8V Vdd for central Bias Circuit	PD	1.8V
18	NC/BJTB	Reserved for future use	PD	Vctrl
19	NC/BJTE	Reserved for future use	PD	3.3V
20	POR	Power on reset input	AI	Logic 0/3.3V
21	SI_ENB	Series interface enable	DI	Logic 0/3.3V
22	SI_CK	Series interface Clock	DI	Logic 0/3.3V
23	SI_DATA	Series interface data I/O	DIO	Logic 0/3.3V
24	SI_RW	Series interface Read/Write	DI	Logic 0/3.3V
25	REFIO	Oscillator Signal Input/Output	DIO	Logic 0/3.3V
26	ENV	RF Chip enable	DI	Logic 0/3.3V '0' all RF circuit off '1' circuit enable is controlled by register
27	VDSI2	1.8V Vdd for series interface	PD	1.8V
28	VDSI3	3.3V Vdd for series interface	PD	3.3V

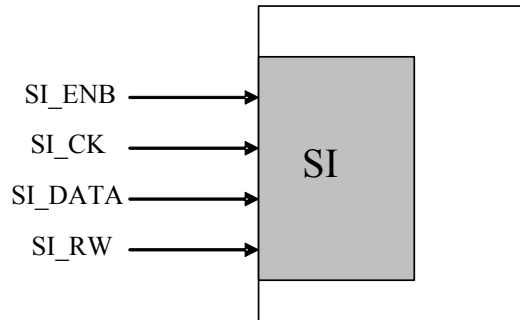


Pin	Pin Name	Function	Pad Tape	DC
29	XSEL	Synthesizer clock source select	DI	Logic 0/3.3V '1' on-chip Osc. '0' off-chip Osc.
30	XENV	Oscillator enable control	DI	Logic 0/3.3V '1' Osc. enable '0' Osc. disable
31	XOUT	Oscillator signal output, Xtal connect terminal	AO	
32	XIN	Xtal connect terminal	AO	
33	VDX	Vdd of oscillator circuit	PD	1.8V
34	GND	Connect to down bond ground	PS	
35	GND	Connect to down bond ground	PS	
36	GND	Connect to down bond ground	PS	
37	GND	Connect to down bond ground	PS	
38	VDRXB	Vdd of RX Baseband and LO Driver	PD	1.8V
39	BOIP	RX Baseband signal Q path output	AO	
40	BOIN	RX Baseband signal Q path output	AO	
41	BOQN	RX Baseband signal I path output	AO	
42	BOQP	RX Baseband signal I path output	AO	
43	RSSI	RSSI Signal Output	AO	
44	VDLO	Vdd of LO Driver and divider	PD	1.8V
45	TQP	TX Baseband Q path input	AO	
46	TQN	TX Baseband Q path input	AO	
47	TIN	TX Baseband I path input	AO	
48	TIP	TX Baseband I path input	AO	

## 6. Serial Interface

The Serial interface provides multiple functions:

### 6.1. Read/Write All Registers

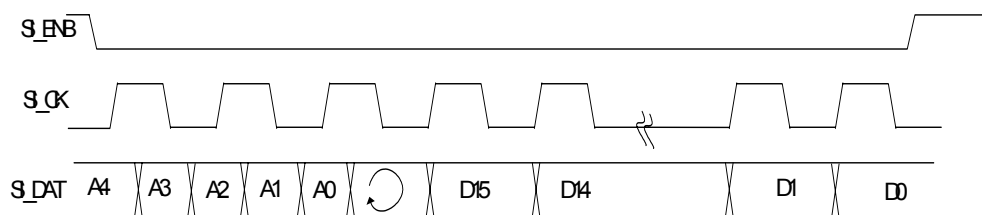


**Figure 3. Read/Write All Registers**

**Table 2. Read/Write All Registers**

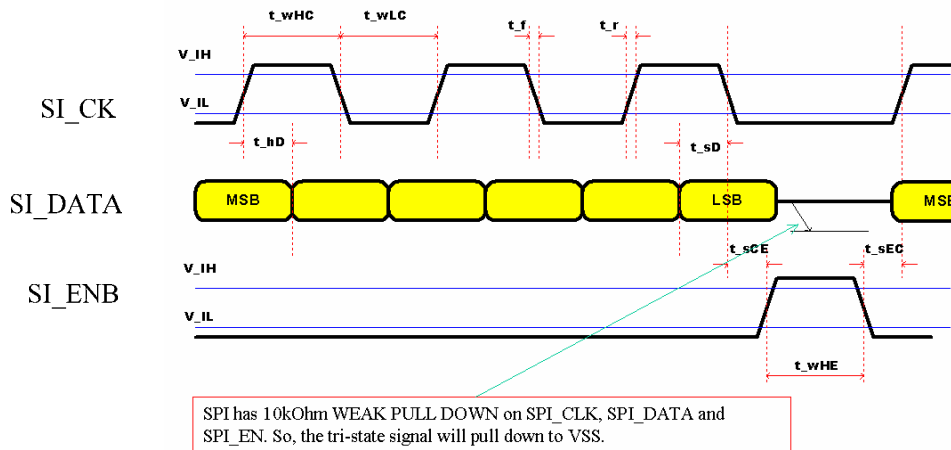
SI Pin	Function
SI_ENB	Series interface enable '1' : disable '0' : enable
SI_CK	Series interface clock come form BB chip
SI_DATA	Register DATA I/O
SI_RW	'1' read data '0' write data

### 6.2. Read Register Data Timing



**Figure 4. Read Register Data Timing**

### 6.3. High Speed Serial Interface Timing



**Figure 5. High Speed Serial Interface Timing**

**Table 3. High Speed Serial Interface Timing**

Parameter	Name	Typ.	Unit
H-input Voltage	V-IH	2 (min), 3.6 (max)	V
L-input Voltage	V-IL	0.5	V
Low pulse width (clock)	t-wLC	12.5	ns
High pulse width (clock)	t-wHC	12.5	ns
High pulse width (enable)	t-wHE	10	ns
Data setup	t-sD	1	ns
Data hold	t-hD	1	ns
Setup time clock-enable	t-sCE	5	ns
Setup time enable-clock	t-sEC	5	ns
Rise, Fall time	t <sub>r</sub> , t <sub>f</sub>	1	ns

## 7. Characteristics

### 7.1. RF Chip Operation Mode Control

**Table 4. RF Chip Operation Mode Control**

Operation Mode	Reg04[14] TX_EN (SW)	Reg04[15] RX_EN (SW)	ENV (HW)	XENV (HW)	Function description
Deep sleep mode	X	X	0	0	All circuit off
Sleep mode	X	X	0	1	Only oscillator on Other circuits off
Deep Standby mode	0	0	1	1	Inactive RX/TX Inactive synthesizer, enable CBC and SI
Standby mode	1	1	1	1	Inactive RX/TX Active synthesizer, CBC and SI
TX Mode	1	0	1	1	Transmitter mode
RX Mode	0	1	1	1	Receiver mode

### 7.2. DC Characteristics

Test temperature=25°C.

**Table 5. DC Specification**

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Power supply voltage		3.3		V	
		2.8		V	
		1.8		V	
Transmit current		100		mA	
Receive current		120		mA	
Standby current (PLL on)		26		mA	
Shut down current		<1		mA	

### 7.3. AC Characteristics

Test temperature=25°C.

**Table 6. AC Specification**

Parameter	Specification			Unit	Condition		
	Min.	Typ.	Max.				
<b>Receiver Overall Specification</b>							
Noise Figure	5.2			dB	Highest Gain		
Input P1dB	-29			dBm	Highest Gain		
Residual DC Offset			20	mV	At LPF2 output		
IQ Imbalance			1.5	dB	Include LO and BB		
				deg			
Supply Voltage							
RF		1.8		V	Regulated		
BB		2.5		V	Regulated		
<b>Transmitter Overall Specification</b>							
Output P1dB			8	dBm	50 ohm load. Highest Gain.		
Output Power	-36		0	dBm	50 ohm load		
TPC range		36		dB	30dB in RF, 6dB per step 6dB in BB controller (RTL8185), 1dB per step		
Unwanted Sideband			36	dBc			
IQ Imbalance			1.5	Deg	Include LO and BB		
				dB			
Carrier Leakage			35	dBc	Highest Gain		
EVM		-30		dB	At Pout= 0 dBm with 54Mbps OFDM signal		
<b>Synthesizer Specification</b>							
Frequency Range	2400		2485	MHz			
Frequency Step		1		MHz			
Loop Bandwidth		60		KHz			
SSB Phase Noise			-90	dBc/Hz			
				100 kHz Offset		-95	dBc/Hz
				1 MHz offset		-115	dBc/Hz
Spurious			-60	dBc			
				Above 10MHz		-70	dBc
LO Drive Level		TBD		Vpp			
Reference Frequency		40		MHz	11g operation		
Settling Time			TBD	μS	Within ±10kHz		
TR Frequency Shift			TBD	kHz			

## 7.4. Measurement Results

1. Transmitter output EVM with 54Mbps OFDM signal. When Pout=0dBm, EVM<-30dB.

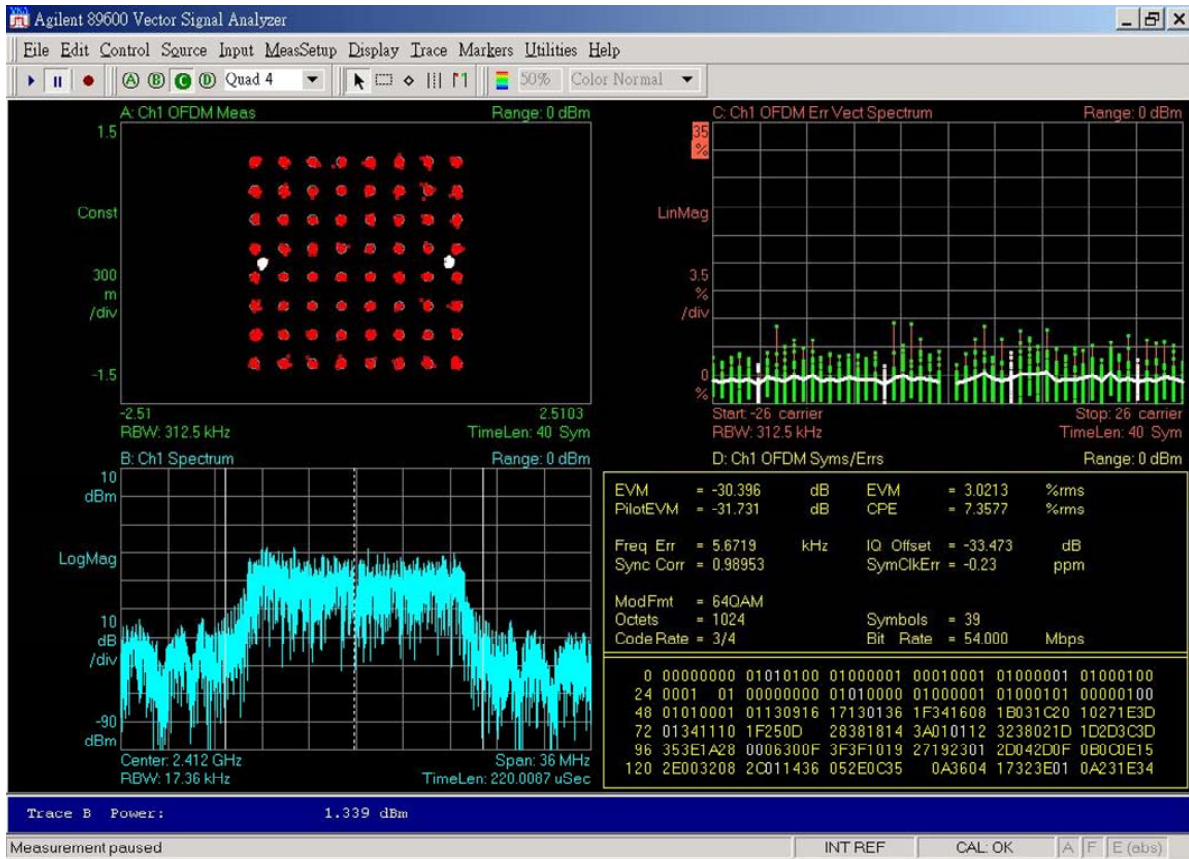


Figure 6. Measurement Results

2. Receiver EVM versus RF input power. EVM=-22.5dB@Pin=-76dBm.

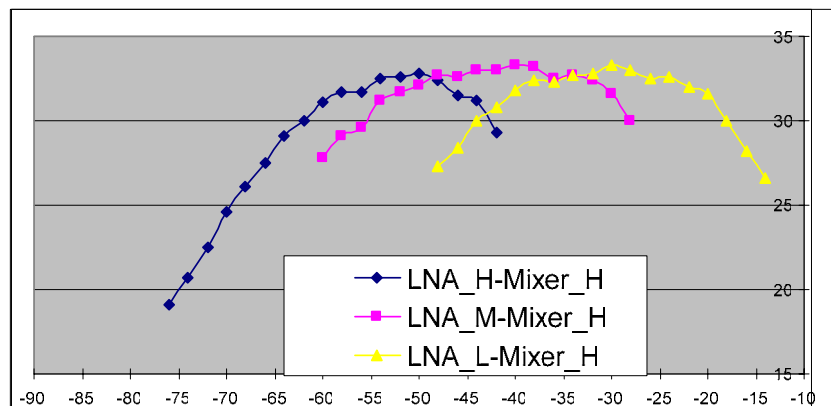
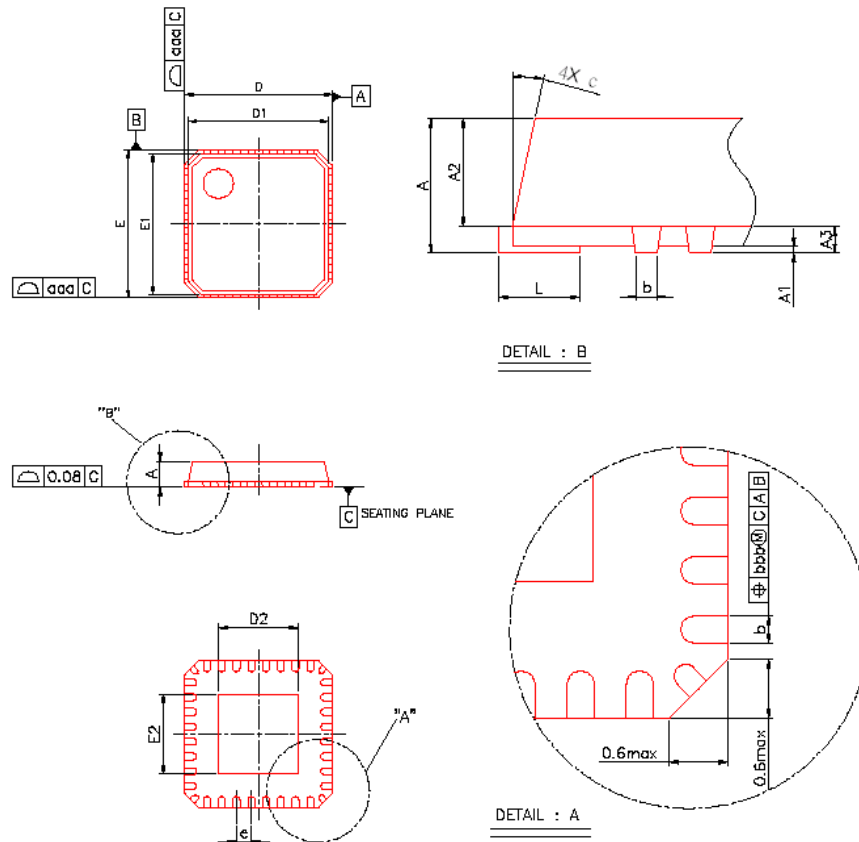


Figure 7. Receiver EVM versus RF input power. EVM=-22.5dB@Pin=-76dBm

## 8. Mechanical Dimensions



SYMBOL	MILLIMETER			INCH		
	MIN.	TYPICAL	MAX.	MIN.	TYPICAL	MAX.
A	0.80	0.85	1.00	0.031	0.033	0.039
A1	0.00	0.02	0.05	0.000	0.001	0.002
A2	---	0.65	1.00	---	0.026	0.039
A3	---	0.20	---	---	0.008	---
b	0.18	0.23	0.30	0.007	0.009	0.012
D	7.00 BSC			0.276 BSC		
D1	6.75 BSC			0.266 BSC		
D2	2.25	4.70	5.25	0.089	0.185	0.207
E	7.00 BSC			0.276 BSC		
E1	6.75 BSC			0.266 BSC		
E2	2.25	4.70	5.25	0.089	0.185	0.207
e	0.50 BSC			0.020 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020
TH	0°	---	12°	0°	---	12°
aaa	---	---	0.25	---	---	0.010
bbb	---	---	0.10	---	---	0.004
chamfer	---	---	0.60	---	---	0.024

TITLE: QFN-48 (7.0x7.0x1.0mm) PACKAGE OUTLINE DRAWING LEADFRAME MATERIAL		
APPROVE	DOC. NO.	
	VERSION	
CHECK	DWG NO.	
	DATE	
REALTEK SEMICONDUCTOR CORP.		

## 9. Ordering Information

**Table 7. Ordering Information**

<b>Part Number</b>	<b>Package</b>	<b>Status</b>
RTL8225	QFN-48	
RTL8225-LF	QFN-48, Lead (Pb)-Free version	

---

**Realtek Semiconductor Corp.****Headquarters**

No. 2, Industry East Road IX, Science-based  
Industrial Park, Hsinchu, 300, Taiwan, R.O.C.

Tel: 886-3-5780211 Fax: 886-3-5776047

[www.realtek.com.tw](http://www.realtek.com.tw)





## Test Report

SILICONWARE PRECISION INDUSTRIES CO., LTD.    Report No. : CE/2004/A3268  
NO. 123, SEC. 3, DA-FONG RD., TANTZU,            Date            : 2004/11/01  
TAICHUNG, TAIWAN, R. O. C.                      Page            : 1 of 2

The following merchandise was (were) submitted and identified by the client as :

Type of Product                                    : LEAD FREE PACKAGE  
Style/Item No                                     : QFN  
Buyer/Order No                                  :  
Sample Received                                : 2004/10/22  
Testing Date                                      : 2004/10/22 TO 2004/11/01

=====  
Test Result                                        : - Please see the next page -

  
Daniel Yeh, M.R. / Operation Manager  
Signed for and on behalf of  
SGS TAIWAN LTD.

The content of this PDF file is in accordance with the original issued reports for reference only. This Test Report cannot be reproduced, except in full, without prior written permission of the Company



## Test Report

SILICONWARE PRECISION INDUSTRIES CO., LTD. Report No. : CE/2004/A3268  
 NO. 123, SEC. 3, DA-FONG RD., TANTZU, Date : 2004/11/01  
 TAICHUNG, TAIWAN, R. O. C. Page : 2 of 2

### Test Result

PART NAME NO.1 : PLEASE REFER TO THE SAMPLE CARD(S).(MIX ALL PARTS)

Test Item (s):	Unit	Method	MDL	Result				
				No.1				
PBBs(Polybrominated biphenyls)(CAS NO:67774-32-7)	%	With reference to USEPA3540 or USEPA3550. Analysis was performed by HPLC/DAD, LC/MS or GC/MS. (prohibited by 2002/95/EC (RoHS), 83/264/EEC and 76/769/EEC)	0.0005	N.D.				
PBBEs(PBDEs)(Polybrominated biphenyl ethers)	%	With reference to USEPA3540 or USEPA3550. Analysis was performed by HPLC/DAD, LC/MS or GC/MS. (prohibited by 2002/95/EC (RoHS), 83/264/EEC and 76/769/EEC)	0.0005	N.D.				

Test Item (s):	Unit	Method	MDL	Result				
				No.1				
Chromium VI (Cr+6)	ppm	As per US EPA 7196A and US EPA 3060A.	2	N.D.				
Cadmium (Cd)	ppm	ICP-AES after as per EN 1122, method B:2001 or other acid digestion.	2	N.D.				
Mercury (Hg)	ppm	ICP-AES after as per US EPA 3052 or other acid digestion.	2	N.D.				
Lead (Pb)	ppm	ICP-AES after as per US EPA 3050B or other acid digestion.	2	N.D.				

NOTE• (1) N.D. = Not detected (<MDL)  
 (2) ppm = mg/kg  
 (3) MDL = Method Detection Limit

The content of this PDF file is in accordance with the original issued reports for reference only. This Test Report cannot be reproduced, except in full, without prior written permission of the Company